SPECIFICATION AMENDMENTS

On page 15, please replace the paragraphs from line 1-25 with the following paragraphs:

~~Fig. 9 is omitted and thus not described herein.~~

Fig. ~~10~~ 9 illustrates a display device capable of decrypting and displaying video signals generated by the display adapter of Fig. 8.

~~Fig. 11 is omitted and thus not described herein.~~

Fig. ~~12~~ 10 illustrates a value mapping circuit of the present invention.

~~Fig. 13 is omitted and thus not described herein.~~

~~Fig. 14 is omitted and thus not described herein.~~

Fig. ~~15~~ 11 illustrates a MUX suitable for use in the value mapping circuit illustrated in Fig. ~~12~~ 10.

On page 42, please replace the paragraph starting at line 11 with the following:

The steps 700~~,~~ are performed by the video signal encryption circuit 806, to encrypt R, G, B video signals as a function of the mapped set A of permutation matrix values~~, are shown in Fig. 9~~.

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On page 44, please replace the paragraphs from line 8 to line 31 with the following:

Having described encryption of the analog R, G, B video signals as performed by the display adapter 848, decoding of the generated composite encrypted R", G' B' signals will now be described with reference to Fig. 9. ~~Figs. 10 and 11.~~

Fig. 9 ~~Fig. 10~~ illustrates a display device 947 which is capable of receiving and decrypting the R', G' B' encrypted analog video signals generated by display adapter 848. The display device 947 includes many components which are the same as, or similar to, those previously discussed with regard to Fig. 6. Such components are identified in Fig. 9 ~~Fig. 10~~ using the same reference numerals as used in Fig. 6 and will not be described again in detail. Note that the display device 947 includes a pseudo random number generator 810 and video signal decryption circuit 906 ~~encryption circuit 806~~ which perform similar functions to those of the like named Fig. 6 components.

Due to implementation issues relating to the decryption circuit 906, and the differences in the implemented analog signal encryption between the Fig. 6 and Fig. 9 ~~Fig. 10~~ embodiments, these circuits may be implemented using hardware and/or software that ~~differs~~ differ from that used to implement the like named circuits found in Fig. 6.

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On page 47, please replace the paragraph starting at line 1 with the following:

~~One~~ In one particular embodiment of the signal decryption process 750 performed by video signal decryption circuit 906 ~~is illustrated in Fig. 11. In Fig. 11~~, the value 4 is not swapped for the value 3, e.g., A3 is not set to A4, and k=3 is used to designate the R signal line. ~~As illustrated the~~ In this particular embodiment, the process begins in start step 752 wherein the set A of mapped matrix values including vectors A1, A2, A3 is received by the decryption circuit 906. The value α may also be received in start step 752.

On page 49, please replace the paragraph starting at line 13 with the following:

The decryption process 750 performed by the video decryption circuit 906 ~~is illustrated in Fig. 11. As illustrated the decryption process~~ begins in start step 752 wherein the encrypted analog video signals R', G' and B' are received as well as the set A of values of the mapped permutation matrix used to encrypt the signals which are to be decrypted. α is also received in step 752 in embodiments where α is not fixed, e.g., set to 1. Operation proceeds from start step 752 to step 754 wherein one of a first through third decrypted video signal $V_{(R', G')}$, $V_{(G',B')}$, $V_{(B',R')}$, is generated for each pair (R',G'), (G',B'), (B', R') of encrypted video signals.

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On page 52, please replace the paragraphs from line 9-25 with the following:

An exemplary value mapping circuit 808, which may be used in the display adapter 848 and display device 947, is illustrated in ~~Fig. 12~~ Fig. 10. The illustrated embodiment assumes that the 9 values in the set A' of permutation matrix values are supplied to the value mapping circuit 808 in parallel, e.g., each on a different line.

The value mapping circuit 808 comprises first through third sets of multiplexers 1002, 1004, 1006 coupled together as shown in ~~Fig. 12~~ Fig. 10. The first set of multiplexers 1002 is responsible for processing the three values comprising A1, corresponding to the first row of the matrix A. Similarly, the second and third sets of multiplexers 1004, 1006 are responsible for processing the values A2, A3 in the second and third rows of the matrix A, respectively.

On page 53, please replace the paragraph starting on line 18 with the following:

The permutation matrix coefficient supplied to the control input of each MUX I010, 1012, 1014 is used to determine whether the signal supplied to the first or second data inputs of each MUX will be output. In the ~~Fig. 12~~ Fig. 10 embodiment, a value of 0 supplied to a MUX control input will result in the signal $+\alpha$, e.g., 1 being output. However, a value of 1 supplied to a MUX control input will result in the signal $-\alpha$, e.g., -1 being output. Thus, MUXes 1010, 1012, 1014 provide a relatively simple way to map

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the set A' of 0 and 1 values to the + α and - α values of the mapped permutation matrix A.

On page 54, please replace the paragraphs from line 1-19 with the following:

~~Fig. 15~~ Fig. 11 illustrates a MUX ~~1500~~ 1100 suitable for use as any one of the MUXes 1010, 1012, 1014. The MUX ~~1500~~ 1100 comprises first and second analog pass gates ~~1502, 1504~~ 1102, 1104. The first analog pass gate ~~1502~~ 1102 has a negated control input while the second analog pass gate ~~1504~~ 1104 has a standard control input. The value + α, e.g., +1, is supplied to the signal input of the first pass gate ~~1502~~ 1102 while the value - α, e.g., -1, is supplied to the signal input of the second pass gate ~~1502~~ 1102. The outputs of the first and second pass gates are both coupled to the output of the MUX ~~1500~~ 1100.

As a result of the negated input on the first pass gate ~~1502~~ 1102, the input signal (+1) to the first pass gate ~~1502~~ 1102will be output by the MUX ~~1500~~ 1100 when the control signal input is a 0. Since the control input of the second pass gate ~~1504~~ 1104 is not negated, the input signal (-1) to the second pass gate ~~1504~~ 1104 will be output by the MUX ~~1500~~ 1100 when the control signal is 1.

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